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10/698,925	10/31/2003	Robert L. Myers	200312732-1	2986

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EXAMINER	
PERVAN, MICHAEL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,925	MYERS, ROBERT L.	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,13-20,22-24 and 27-29* is/are rejected.

7)☒ Claim(s) *8,11,12,21,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 9-10, 13-14, 24 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura et al (US 6,175,351).

In regards to claim 1, Matsuura discloses a method for transmitting digital video over an analog interface comprising:

accessing digital video data having a number of bits per color per pixel (col. 12, lines 30-33; in order to encode (convert) the digital data to analog data, the D/A encoder (converter) must have access to the digital data);

encoding said digital video data such that analog compatibility standards are preserved (col. 12, lines 30-33; since the digital data gets encoded (converted) into analog data for display, the analog compatibility is preserved); and

transmitting said encoded digital video data over an analog interface (col. 12, lines 33-35; the encoded (converted) digital data is transferred via the analog interface (data transfer circuit)).

Matsuura does not disclose said bits per color per pixel are encoded to an amplitude level.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight.

In regards to claim 2, Matsuura does not disclose the method as recited in claim 1 further comprising: encoding six bits per color per pixel of said digital video data.

However, since there is no benefit or advantage described in the specification for choosing six bits, the examiner believes this to be a designer's choice.

In regards to claim 3, Matsuura does not disclose the method as recited in claim 1 further comprising: encoding a plurality of bits of said digital video data to one of eight available amplitude levels.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

In regards to claim 4, Matsuura does not disclose the method as recited in claim 3 further comprising: encoding said plurality of bits of said digital video data to an amplitude level between 0.0 volts and 0.7 volts.

However, the values claimed are arbitrary and since no viable advantage or benefit is described in the specification, the examiner believes this to be a designer's choice.

In regards to claim 5, Matsuura discloses the method as recited in claim 1 further comprising: encoding said digital video data such that each pixel is represented by three bits (col. 12, lines 60-64; the digital video data of each pixel is represented by three bits (R,G,B)).

Matsuura does not disclose wherein each of said three bits are encoded to one of eight available levels of amplitude.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

In regards to claim 9, Matsuura does not disclose the method as recited in claim 1 further comprising: decoding said amplitude level to a brightness level compatible with a fixed-format video display.

However, it would be obvious to one of ordinary skill in the art to decode said amplitude levels to brightness levels since in order to produce different colors on a display different levels of R, G and B are combined to produce various colors of the gamut. For example, the highest amplitude level for R and the lowest amplitude level for G and B would produce the color Red.

In regards to claim 10, a system for transmitting digital video data over an analog video interface comprising:

an input for receiving digital video data comprising a number of bits per color per pixel (col. 12, lines 28-33; an input (time-axis modulation circuit) receives digital video data comprising a number of bits per color per pixel (R,G,B));

a digital to analog video encoder coupled to said input for encoding said digital video data such that analog compatibility standards are preserved (col. 12, lines 30-33; since the digital data gets encoded (converted) into analog data for display, the analog compatibility is preserved); and

an output coupled to said digital to analog video encoder configured to communicatively couple to an analog video transmission line for transmitting said encoded digital video data (col. 12, lines 33-35; the encoded (converted) digital data is transferred via the analog interface (data transfer circuit)).

Matsuura does not disclose said bits per color per pixel are encoded to an amplitude level.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight.

In regards to claim 13, Matsuura does not disclose the system as recited in claim 10 wherein said digital to analog video encoder encodes said bits per color per pixel to one of eight distinguishable amplitude levels.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of

available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

In regards to claim 14, the system as recited in claim 10 wherein said digital to analog video encoder encodes three bits per said color per said pixel and wherein said three bits are encoded to an amplitude level between 0.0 volts and 0.7 volts.

However, the values claimed are arbitrary and since no viable advantage or benefit is described in the specification, the examiner believes this to be a designer's choice.

In regards to claim 24, it recites claim limitations similar to those of claim 10 and is therefore rejected for the same reasons.

In regards to claim 27, Matsuura does not disclose the encoder as recited in claim 24 wherein said encoder module encodes said bits per color per pixel to one of eight distinguishable amplitude levels.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

In regards to claim 28, Matsuura does not disclose the encoder as recited in claim 24 wherein said encoder module encodes three bits per said color per said pixel and wherein said three bits are encoded to an amplitude level between 0.0 volts and 0.7 volts.

However, the values claimed are arbitrary and since no viable advantage or benefit is described in the specification, the examiner believes this to be a designer's choice.

3. Claims 6-7, 16-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura et al in view of Kim et al (US 6,614,424).

In regards to claim 6, Matsuura does not disclose the method as recited in claim 1 further comprising: separating even bits and odd bits of said number of bits per color per pixel.

Kim discloses separating even bits and odd bits of said number of bits per color per pixel (col. 6, lines 6-10; bits per color per pixel (RD, GD, BD) are separated into even and odd bits (RDBe, GDBe, BDBe, RDBo, GDBo, BDBo)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, separating even bits and odd bits of said bits per color per pixel, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 7, Matsuura does not disclose the method as recited in claim 6 further comprising: transmitting said even bits and said odd bits on successive cycles of a symbol-rate clock.

Kim discloses transmitting said even bits and said odd bits on successive cycles of a symbol-rate clock (Fig. 10 and col. 6, lines 17-22; as can be seen in the drawing, the even (RDBe, GDBe, BDBe) and odd bits (RDBo, GDBo, BDBo) are transferred in successive symbol-rate clock (MCLK)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, transmitting said even bits and said odd bits on successive cycles of a symbol-rate clock, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 16, Matsuura does not disclose the system as recited in claim 15 further comprising: a symbol-rate clock coupled to said output configured such that said even and said odd bits can be transmitted in successive clock cycle of said symbol-rate clock.

Kim discloses a symbol-rate clock coupled to said output configured such that said even and said odd bits can be transmitted in successive clock cycle of said symbol-rate clock (Fig. 10 and col. 6, lines 17-22; as can be seen in the drawing, the even (RDBe, GDBe, BDBe) and odd bits (RDBo, GDBo, BDBo) are transferred in successive symbol-rate clock (MCLK)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, transmitting said even bits and said odd bits on successive cycles of a symbol-rate clock, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 17, Matsuura discloses a method for encoding digital video data to an analog compatible format comprising:

accessing a plurality of bits per color per pixel of digital video data (col. 12, lines 30-33; in order to encode (convert) the digital data to analog data, the D/A encoder (converter) must have access to the digital data);

Matsuura does not disclose encoding said bits per color per pixel to one of a plurality of available amplitude levels, separating said plurality of bits per color per pixel into even bits and odd bits and transmitting said even bits and said odd bits in successive clock cycles of a symbol rate clock.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight.

Matsuura does not disclose separating said plurality of bits per color per pixel into even bits and odd bits and transmitting said even bits and said odd bits in successive clock cycles of a symbol rate clock.

Kim discloses separating said plurality of bits per color per pixel into even bits and odd bits (col. 6, lines 6-10; bits per color per pixel (RD, GD, BD) are separated into even and odd bits (RDBe, GDBe, BDBe, RDBo, GDBo, BDBo)) and transmitting said even bits and said odd bits in successive clock cycles of a symbol rate clock (Fig. 10 and col. 6, lines 17-22; as can be seen in the drawing, the even (RDBe, GDBe, BDBe) and odd bits (RDBo, GDBo, BDBo) are transferred in successive symbol-rate clock (MCLK)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, transmitting said even bits and said odd bits on successive cycles of a symbol-rate clock, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 18, Matsuura does not disclose the method as recited in claim 17 further comprising: restricting said available amplitude levels to eight levels.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

In regards to claim 19, Matsuura does not disclose the method as recited in claim 18 further comprising: encoding a first set of bits of said bits per color per pixel to one of said eight available amplitude levels and transmitting said encoded first set of bits of said bits per color per pixel.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

Matsuura does not disclose transmitting said encoded first set of bits of said bits per color per pixel.

Kim discloses transmitting said encoded first set of bits of said bits per color per pixel (Fig. 10 and col. 6, lines 17-22; as can be seen in the drawing, the even (RDBe, GDBe, BDBe) and odd bits (RDBo, GDBo, BDBo) are transferred in successive symbol-rate clock (MCLK)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, transmitting said encoded first set of bits of said bits per color per pixel, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 20, Matsuura does not disclose the method as recited in claim 19 further comprising: encoding a second set of bits of said bits per color per pixel to one of said eight available amplitude levels and transmitting said encoded second set of bits of said bits per color per pixel.

However, it would be obvious to one of ordinary skill in the art to encode said bits to an amplitude level. For example, three bits would give eight different amplitude levels since two raised to the power of three gives eight. Therefore, the number of available amplitude levels is determined by the number of bits and is believed to be a designer's choice.

Matsuura does not disclose transmitting said encoded second set of bits of said bits per color per pixel.

Kim discloses transmitting said encoded second set of bits of said bits per color per pixel (Fig. 10 and col. 6, lines 17-22; as can be seen in the drawing, the even (RDBe, GDBe, BDBe) and odd bits (RDBo, GDBo, BDBo) are transferred in successive symbol-rate clock (MCLK)).

It would have been obvious at the time of invention to modify Matsuura with the teachings of Kim, transmitting said encoded second set of bits of said bits per color per

pixel, by incorporating the teachings of Kim into the device of Matsuura because it would reduce the electromagnetic interference (col. 1, lines 7-10).

In regards to claim 22, Matsuura does not disclose the method as recited in claim 17 further comprising: decoding said amplitude level to a brightness level compatible with a fixed-format video display.

However, it would be obvious to one skilled in the art to decode said amplitude levels to brightness levels since in order to produce different colors on a display different levels of R, G and B are combined to produce various colors of the gamut. For example, the highest amplitude level for R and the lowest amplitude level for G and B would produce the color Red.

In regards to claim 23, Matsuura does not disclose the method as recited in claim 17 further comprising: encoding said bits of said bits per color per pixel of said digital video data to an amplitude level between 0.0 volts and 0.7 volts.

However, the values claimed are arbitrary and since no viable advantage or benefit is described in the specification, the examiner believes this to be a designer's choice.

4. Claims 15 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura et al in view of Kim et al in further view of Koh (US 5,534,883).

In regards to claim 15, Matsuura and Kim do not disclose the system as recited in claim 10 further comprising: a multiplexer coupled to said digital to analog video encoder for separating said bits per color per pixel into even and odd bits.

Koh discloses a multiplexer coupled to said digital to analog video encoder for separating said bits per color per pixel into even and odd bits (col. 5, lines 32-37; the multiplexer separates the even and odd bits of Kim based on the timing of the display).

It would have been obvious at the time of invention to modify Matsuura and Kim with the teachings of Koh, multiplexer coupled to said digital to analog video encoder for separating said bits per color per pixel into even and odd bits, by incorporating the multiplexer of Koh into the device of Matsuura and Kim because it simplifies the circuitry and allows for serial communication of even and odd bits.

In regards to claim 29, Matsuura and Kim do not disclose the encoder as recited in claim 24 further comprising: a multiplexer coupled to said digital to encoder module for separating said bits per color per pixel into even and odd bits.

Koh discloses a multiplexer coupled to said digital to encoder module for separating said bits per color per pixel into even and odd bits (col. 5, lines 32-37; the multiplexer separates the even and odd bits of Kim based on the timing of the display).

It would have been obvious at the time of invention to modify Matsuura and Kim with the teachings of Koh, multiplexer coupled to said digital to analog video encoder for separating said bits per color per pixel into even and odd bits, by incorporating the multiplexer of Koh into the device of Matsuura and Kim because it simplifies the circuitry and allows for serial communication of even and odd bits.

Allowable Subject Matter

5. Claims 8, 11, 12, 21, and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claims 8, 11, 21 and 25, they recite among transmitting even bits and odd bits over a New Analog Video Interface (NAVI). The examiner was unable to find a reference or combination of references, which would teach said limitation as described by the specification.

Response to Arguments

6. Applicant's arguments filed March 5, 2007 have been fully considered but they are not persuasive.

Applicant (on page 4 of argument) argues that since Matsuura is silent with respect to "a number of bits per color per pixel", Matsuura cannot teach or suggest said limitation and in fact teaches away from "said bits per color per pixel are encoded to an amplitude level". Examiner respectfully disagrees.

As can be seen in Figure 1, each color analog signal (R, G, B) has an A/D converter (20) followed by three memory units (30). Each analog signal is converted (encoded) into a digital signal (number of bits). This digital signal is then passed to the memory units, which then send the digital signal to the Time-axis modulation circuit. From the Time-axis modulation circuit, the digital signal is then sent to a number of D/A converters, which convert (encode) the digital signal (number of bits) back into an

analog signal (representing continuous amplitude levels). In order for the digital signal to be converted (encoded) back to an analog signal, the D/A converters must have access to the digital signal. Therefore, the D/A converters access the digital signal and convert (encode) it to an analog signal.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP

May 18, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER